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Gate-Controlled Energy Barrier at a Graphene/Molecular Semiconductor Junction

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The formation of an energy-barrier at a metal/molecular semiconductor junction is a universal phenomenon which limits the performance of many molecular semiconductor-based electronic devices, from field-effect transistors to light-emitting diodes. In general, a specific metal/molecular semiconductor combination of materials leads to a fixed energy-barrier. However, in this work, a graphene/C_{60} vertical field-effect transistor is presented in which control of the interfacial energy-barrier is demonstrated, such that the junction switches from a highly rectifying diode at negative gate voltages to a highly conductive nonrectifying behavior at positive gate voltages and at room temperature. From the experimental data, an energy-barrier modulation of up to 660 meV, a transconductance of up to five orders of magnitude, and a gate-modulated photocurrent are extracted. The ability to tune the graphene/molecular semiconductor energy-barrier provides a promising route toward novel, high performance molecular devices.

1. Introduction

The formation of an energy barrier at a metal/molecular semiconductor junction is both a ubiquitous phenomenon as well as the subject of intense research in order to improve the performance of molecular semiconductor-based electronic and optoelectronic devices.[1–7] For these devices, a junction with a large energy barrier provides rectification, leading to a diode behavior, whereas a relatively small energy barrier provides a highly conductive nonrectifying behavior, resulting in efficient carrier injection into (or extraction from) the molecular semiconductor.[4] Typically, a specific metal/molecular semiconductor combination leads to a fixed energy barrier, which crucially determines the device performance and efficiency;[8–10] therefore, the possibility of a gate-controlled energy barrier is very appealing from the point of view of possible advanced applications.

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Graphene,[11] a one-atom thick zero band gap semiconductor has allowed the development of new electronic device schemes such as the graphene-barristor,[12] the graphene-vertical-field-effect-transistor (VFET),[13–16] and the graphene-base hot electron transistor.[17] In organic electronics, graphene can be an ideal choice to use as the injector (or source) electrode for a VFET since its Fermi level, its corresponding work function and its available low density of states (DOS)[18] can all be easily modulated, providing a tunable energy barrier which eventually controls the device operation. In addition, the electric field produced by a gate electrode will extend into the organic semiconductor, as the monolayer thickness of graphene is insufficient to fully screen it.[13,19]

In order to increase the performance of organic thin film transistors (OTFT) compared with the inorganic counterparts, a unique vertical architecture with a molecular semiconductor (C_{60}) was first demonstrated using a thin and rough (with a roughness comparable to the thickness) metal electrode.[20] A clear advantage of the vertical over the lateral organic transistor geometry is that the channel length is controlled by the thickness of the organic layer and the devices can be downsized in both the lateral and the vertical directions. In the case of a perforated metallic source electrode, the electric field can directly access the metal/organic interface which causes the energy level realignment (similar to the band bending in inorganic semiconductor) in the organic semiconductor. Although Ma and Yang have reported a large on/off current ratio ($\approx 10^6$), the high DOS and the fixed work function of the metallic electrode (injector) limits its application to a few organic semiconductors.[20] Later on, Liu et al. introduced a carbon nanotube-based source electrode with low DOS in organic VFETs for a wide range of organic semiconductors.[21] Carbon nanotubes allow new mechanisms for transistor operation such as the tuning of the gate modulated energy barrier. Graphene, similar to carbon nanotubes in its electrical and mechanical properties, has additional advantages over them due to the large-scale availability (chemical vapor deposition (CVD)-grown graphene) of chemically inert high quality 2D surfaces.[14,22]

On the other hand, fullerene (C_{60}) is one of the most widely studied molecular semiconductors[2,5,20,23–25] and a common choice as an active media for transistors. C_{60} has an energy gap (E_g = 1.7 eV), between its highest occupied molecular orbital

(HOMO: 6.2 eV) and the lowest unoccupied molecular orbital (LUMO: 4.5 eV), larger than the band gap of conventional inorganic semiconductors, e.g., Si (E_g = 1.12 eV)[12] and MoS_2 (bulk E_g = 1.29 eV)[13]. As the C_{60} LUMO level is close to the work function of graphene,[18] it is interesting to study the electron injection properties of a graphene/C_{60} junction. Therefore, in general the graphene/C_{60} junctions are a very promising combination for the fabrication of organic VFETs, which should also serve as useful components for logic circuits.

In this work, we implement a graphene/C_{60} junction that shows a gate tunable energy barrier. The junction acts as a highly rectifying diode for negative gate voltages and controllably switches to a nonrectifying low resistance junction for positive gate voltages. From our experimental data, we extract a zero bias energy barrier modulation up to 0.66 eV (from 0.88 to 0.22 eV). The control over the graphene/C_{60} junction energy barrier by the applied gate voltage leads to the operation of a graphene/C_{60}/metal VFET with a measured current on/off ratio of up to five orders of magnitude at room temperature (RT). Moreover, we report a gate-controlled photo-transistor in which the photocurrent is exponentially dependent on the graphene/C_{60} junction energy barrier. Our ability to modulate such an energy barrier provides a promising route toward molecular semiconductor-based devices combining the properties of a rectifying diode and of a nonrectifying low resistance junction in a single device.

Figure 1a,b shows a schematic diagram of the graphene/C_{60} junction-based VFET and a cross-sectional scheme of the device, respectively. The fabrication steps are explained in detail in the Experimental Section. Briefly, a single layer graphene, grown by CVD [26] is transferred onto a Si^{++}/SiO_2 substrate. The highly doped Si and the 300 nm thick thermal SiO_2 layer act as a gate electrode (G) and a gate dielectric, respectively. The graphene is then lithographically patterned and etched by oxygen plasma into several 2 mm long and 10 µm wide strips. Ti/Au (2.5 nm/40 nm) layers are then deposited by e-beam evaporation at the two ends of each graphene strip for contacts (S, D*). Next, a 280 nm thick C_{60} layer is evaporated on graphene in ultrahigh vacuum (UHV) conditions. A cross-bar geometry, realized through a shadow mask, defines a graphene/C_{60} junction area of 1 mm × 10 µm. Finally, a 30 nm thick layer of either Al or Cu is deposited on top of C_{60} for the collector or drain contact (D). Both metals have work functions closely matching to the C_{60} LUMO energy level and are thus an optimal choice for electron transport. The top view of an actual device is shown in Figure 1c, where the graphene strip is indicated inside the dotted lines. The active device area is considered to be confined to the overlapping

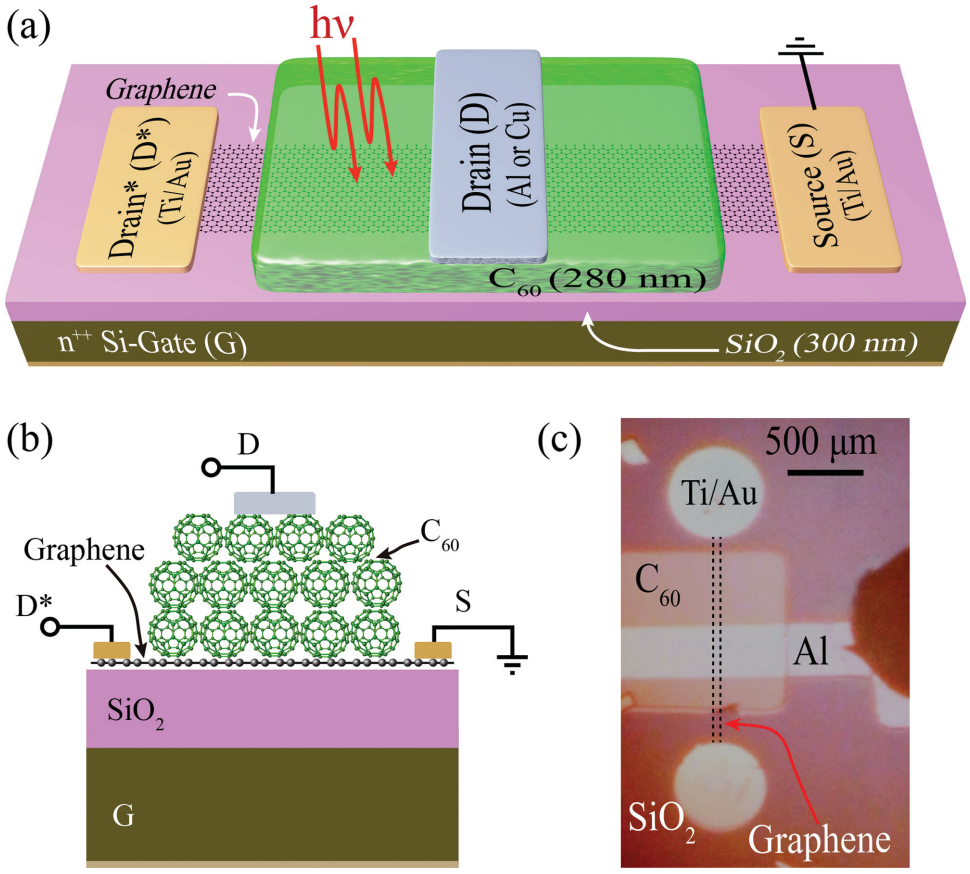

Figure 1. a) Schematic diagram of our device, which acts as a lateral graphene field effect transistor as well as a graphene/C_{60}-based vertical field effect transistor. CVD-grown graphene is transferred on a Si/SiO_2 substrate and subsequently patterned. Ti/Au contacts and C_{60} are then separately evaporated. Finally, either Al or Cu is deposited on top of C_{60} for the collector (drain) contact. b) Cross-sectional schematic view of the device. c) Optical microscopy image of a typical graphene/C_{60}/metal device.

area (10×300 μm^2) between the bottom graphene and the top drain (D) electrode.

2. Results and Discussion

We organize the experimental results in the following four parts. First, we briefly discuss the graphene field effect transistor (graphene-FET) with and without the presence of a C_{60} layer above and the surface charge carrier mobility in the graphene. Second, we measure the gate-controlled energy barrier between graphene and C_{60} junction. Third, we show the operation of a VFET based on the graphene/C_{60} energy barrier modulation. Fourth and last, we describe the gate-controlled photocurrent measurement in the graphene/C_{60}/metal device. All our results reveal the exceptional potential of graphene as a universal electrode, replacing metals and carbon nanotubes for organic electronic and optoelectronic devices.

In order to investigate the charge transfer between the monolayer graphene and the organic semiconductor, we briefly discuss the effect of a thick C_{60} layer on the transport of the graphene-FET. **Figure 2**a,b shows the dependence of the square resistance of the graphene strip (R_{sq}, measured between S and D*) versus the gate-source voltage (V_{GS}), before depositing the C_{60} film and after fabricating the complete device. Initially, the graphene is highly p-doped, i.e., its charge neutrality point (CNP) is visible at positive gate voltage and presents a considerable variability in the position of its CNP (within 45–90 V). In the examples presented in Figure 2, CNPs are found at V_{GS} of 48 and 80 V. Such p-doping is common when CVD-graphene is transferred onto Si/SiO_2 substrates.[27] The addition of a C_{60} layer shifts the position of the CNP to lower V_{GS} (31 and 34 V for graphene/C_{60}/Al and graphene/C_{60}/Cu devices, respectively), and, more importantly, it effectively reduces the dispersion. Such reduction on the graphene doping can be understood by considering the formation of an electrical dipole at the graphene/C_{60} junction due to charge transfer.[28–30] We assume that there is no influence of the top metallic electrodes (Al and Cu) present above the C_{60} layer in case of graphene-FET measurements, which seems logical due to thick molecular layer employed. In every case studied, the square resistance of graphene does not vary significantly after the C_{60} deposition, indicating that other properties of graphene apart from the doping remain nearly unchanged and that there is not any evidence of chemical reaction at the interface.

In order to extract the carrier mobility in the pristine graphene strip without C_{60}, we first estimate the surface charge carrier density (n) induced by the gate voltage as

$$n = C_j q^{-1} |V_{GS} - V_{CNP}| \quad (1)$$

where $C_j = 12$ nF cm^{-2} is the gate capacitance per unit area for a 300 nm thick SiO_2 layer, V_{CNP} is the voltage corresponding to the CNP, and q is the elementary charge.[30] We note that Equation (1) is strictly valid only in the case of an ideal capacitor, for which all the electric field is confined in between the gate and the graphene strip. As soon as we consider a nonperfect electrical screening at the graphene/C_{60} interface, a redistribution of the carrier density will emerge so that $n_{graphene} < n$ carriers will populate the graphene while $n_{C_{60}} = n - n_{graphene}$ carriers will be induced in the first layers of C_{60}. It is worth noting that Equation (1) provides a valid upper limit for the induced carriers and it is useful in order to compare the performance of our device with similar ones in the literature.

From the R_{sq}–V_{GS} measurement performed on the graphene strip we calculate the surface charge carrier mobility, $\mu = 1/nqR_{sq} \approx 3000$ cm^2 V^{-1} s^{-1} at RT. We extract such mobility at a specific carrier density $n \approx 10^{12}$ cm^{-2} where the first derivative of the R_{sq} curve with V_{GS} shows a maximum (for the specific case of the graphene layer with $V_{CNP} \approx 48$ V the deflection point is at 35 V).[31] The typical measured mobilities for our graphene-FETs are always in excess of 1000 cm^2 V^{-1} s^{-1}, which indicates the quality of the CVD graphene films.[27,32]

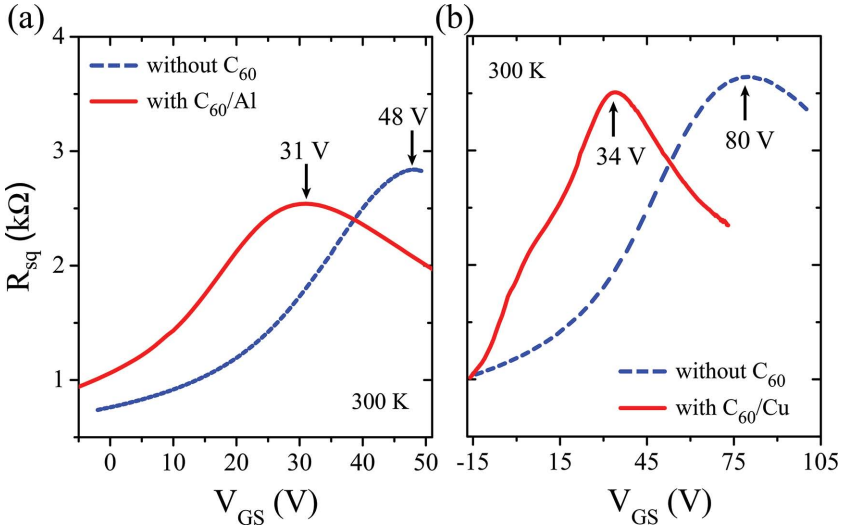

Figure 2. Electrical transport characteristics of the graphene field effect transistors with and without a C_{60} layer on top of graphene for a) graphene/C_{60}/Al and b) graphene/C_{60}/Cu, respectively. The graphene square resistance (R_{sq}) is plotted with respect to the gate-source voltage (V_{GS}) at room temperature (300 K) in all cases.

Figure 3a represents the rigid-band approximation energy diagram in which the work functions of each of the materials are individually plotted with respect to the vacuum level. Figure 3b,c is used to illustrate the device operation at both negative and positive V_{GS} with grounded graphene, respectively. A negative V_{GS} shifts the Fermi-level of the graphene downwards, effectively increasing the graphene/C_{60} junction energy barrier (ϕ_B) for electrons. In the case when the graphene/C_{60} junction is under a negative V_{DS} (solid line), electrons can easily move from the top metal contact to the graphene after passing the graphene/C_{60} junction energy barrier (similar to the forward bias condition of a diode). However, a large ϕ_B will impede the reverse flow of electrons (dotted line) in case of a positive V_{DS}, as the electron has to overcome the large barrier, which can be denoted as the "off" state of

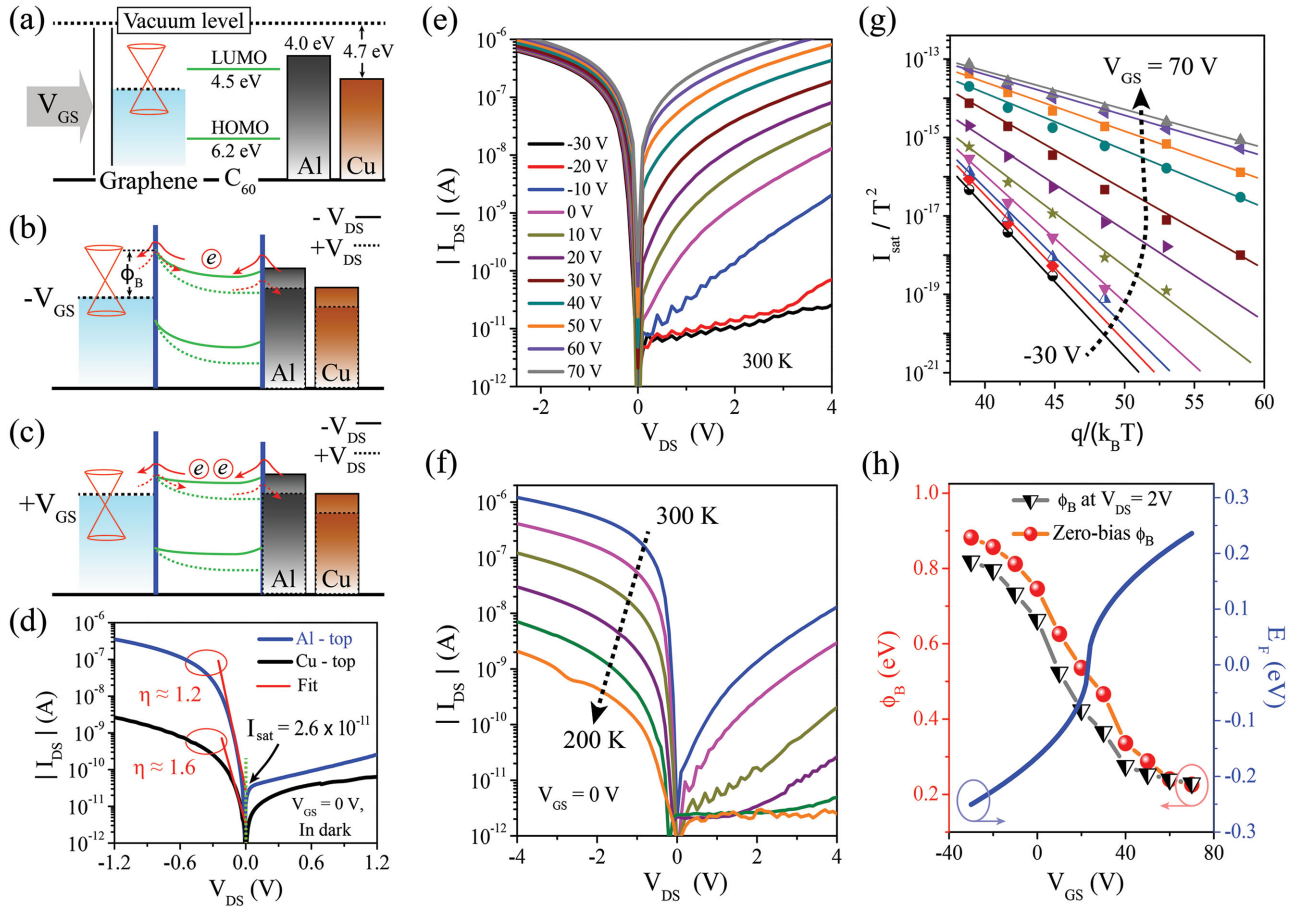

Figure 3. a) Rigid-band approximation energy diagram of a transistor, representing the hole-doped graphene strip, the molecular levels of C_{60} and the work function of the collector metal (Al, Cu). The same energy diagram under b) negative V_{GS} and c) positive V_{GS} with grounded graphene film under negative V_{DS} (solid) and positive V_{DS} (dashed), respectively. d) Current–voltage characteristics of the graphene/C_{60} interface at zero V_{GS}, at RT and in dark for both Al and Cu top contacts. e) I_{DS}–V_{DS} diode characteristics for different V_{GS} (step of 10 V) in graphene/C_{60}/Al-based transistor. f) Temperature dependent (step of 20 K) I_{DS}–V_{DS} output characteristics at zero V_{GS}. g) The zero-bias saturation current, I_{sat} is determined by fitting I_{DS} at negative V_{DS} regime using Equation (2) at various temperatures and gate voltages (step of 10 V) [an example is shown in (d)]. I_{sat}/T^2 is plotted against $q/(k_BT)$ and fitted by Equation (3) to extract the zero-bias energy barriers which are h) plotted at different V_{GS}. Energy barriers at V_{DS} of 2 V are also extracted and plotted in (h). The changes in graphene Fermi energy at similar V_{GS} are estimated by Equations (1) and (4) (see main text for the considerations on the validity of these equations) and are plotted (for $V_{CNP} \approx 23$ V) in the right *y*-axis.

the transistor. In case of a positive V_{GS}, the graphene Fermi-level shifts upwards while more electrons will be induced in the first few monolayers of C_{60} (due to the weak screening of the electric field by the graphene and the fringe field contribution near its edges). This effect not only reduces the graphene/C_{60} junction ϕ_B but also modifies the C_{60} energy levels alignment with respect to graphene, such that the electron transport (both injection and extraction) will be much easier for both positive and negative V_{DS} and the rectification of the graphene/C_{60} junction will be diminished. We highlight the fact that the energy barrier modulation will only be at the graphene/C_{60} junction whereas the C_{60}/metal junction (top contact) will act as a fixed barrier without any change at different V_{GS}. This is mainly caused by the large DOS in conventional metals, which requires an exceedingly large amount of induced charges to modulate their Fermi-level.[14]

Figure 3d shows the current–voltage (I_{DS}–V_{DS}) characteristics of both graphene/C_{60}/Al and graphene/C_{60}/Cu devices, in the dark and without applying any V_{GS}. As indicated above, the diodes are considered to be in forward bias when a negative V_{DS} is applied, i.e., electrons are being injected from the LUMO level of C_{60} to graphene whereas a positive V_{DS} changes the diode operation into reverse bias condition. Rectification is clearly observed for both metal contacts in its forward bias operation, although the effect is larger for the case of the Al than for the Cu electrode. The discrepancy between the two diodes is likely due to the difference in chemical processes at the interface between the C_{60} LUMO level and the different top metal electrodes with different work functions. To estimate the diode quality, we use the following equation which accounts for both thermionic emission and tunneling transport through the graphene/C_{60} junction[13,33]

$$I_{DS} = I_{sat}\left[exp\left(\frac{qV_{DS}}{\eta k_B T}\right) - 1\right] \approx I_{sat}\left[exp\left(\frac{qV_{DS}}{\eta k_B T}\right)\right] \quad (2)$$

where I_{sat} is the saturation current (at zero bias), k_B is the Boltzmann constant, T is the temperature, and η is the ideality factor. η determines the quality of the rectifying interface; if $\eta = 1$, the diode would be ideal and the transport will be only mediated by thermionic emission (electrons will surmount the barrier rather than going through the barrier).[33] Fittings of I_{DS} in the forward bias region of low V_{DS} ($|V_{DS}| > 100$ mV) deliver values for $\eta \approx 1.2$ for the graphene/C_{60}/Al diode and $\eta \approx 1.6$ for the graphene/C_{60}/Cu diode, respectively. Similar values have been reported for graphene junctions with other standard semiconductors.[12,13,34,35] The I_{sat} values are then extracted from the same fit by Equation (2) as the extrapolated current at $V_{DS} = 0$ (from Figure 3d, $I_{sat} = 2.6 \times 10^{-11}$ A for graphene/C_{60}/Al diode), and are used afterwards for the energy barrier extraction.

The I_{DS}–V_{DS} characteristics at different V_{GS} and at RT are shown in Figure 3e for the graphene/C_{60}/Al diode. Large rectification (defined as the ratio between the forward current at $V_{DS} = -2$ V and the reverse current at $V_{DS} = +2$ V) of up to five orders of magnitude can be obtained for large negative voltages (at $V_{GS} = -30$ V), gradually decreasing to zero (symmetric I_{DS}–V_{DS} curve) when V_{GS} moves to positive values. Increasing the positive gate voltage increases the reverse current of the diode, which indicates that the VFET in reverse bias operation behaves as an n-channel transistor. The effect of large modulation in I_{DS} by V_{GS} at positive V_{DS} is mainly governed by the large change in graphene/C_{60} junction energy barrier (ϕ_B). The change in the energy barrier can be obtained by the temperature dependent measurements of the I_{DS}–V_{DS} characteristics at several fixed gate voltages [Figure 3f represents temperature dependent I_{DS}–V_{DS} at zero gate voltage] and by fitting the results to the Richardson–Dushman thermionic emission theory,[22,33]

$$I_{DS} = AA^{*}T^{2}\exp\left(-\frac{q\phi_B}{k_BT}\right) \quad (3)$$

where A is the junction area and A^* is the effective Richardson constant (an unknown parameter for C_{60}). The ϕ_B can be extracted as the zero-bias energy barrier in case of I_{sat} instead of I_{DS}[13] in Equation (3). A biased energy barrier can also be extracted after directly using the experimental values of I_{DS} in Equation (3) at a large positive V_{DS} (here at $V_{DS} = 2$ V).[12,22] The zero-bias energy barrier, considered to be more fundamental since it does not involve any voltage drop across the junction, is often very challenging to determine as it requires I_{sat} from another fitting. In our case, we report both obtained values of ϕ_B for a fair comparison. For zero-bias ϕ_B, I_{sat} is extracted at different temperatures and at several V_{GS} after fitting I_{DS} at low forward bias regime by Equation (2) [an example is shown in Figure 3d]. Figure 3g shows the plots of I_{sat}/T^2 versus $q/(k_BT)$ at various V_{GS}. ϕ_B is then extracted from the slope of each curve and is further plotted in Figure 3h with respect to the applied V_{GS}. At low temperature and at large negative V_{GS}, the data points largely deviate from the fitting in Figure 3g due to a large change in nonideality of the diode and are excluded from the fitting. At a large negative V_{GS} of −30 V, the zero-bias barrier height is as large as 0.88 eV which gradually decreases to 0.22 eV for a large positive V_{GS} of 70 V. The gate modulation of graphene/C_{60} junction energy barrier is more than three times larger than the previously reported on other graphene-VFETs with Si[12] and MoS_2.[13] The biased ϕ_B is similarly extracted (not shown here) from the directly measured I_{DS} at $V_{DS} = 2$ V and it is plotted in Figure 3h. ϕ_B at $V_{DS} = 2$ V shows a similar trend to zero-bias ϕ_B and varies from 0.82 to 0.23 eV in the same V_{GS} range. To address such a large change in ϕ_B, we calculate the shift in the graphene Fermi-level due to the change in carrier concentration (n, which we estimate using Equation (1) assuming that the large majority of the induced carriers lies in the graphene) at different V_{GS} as

$$E_F = \pm\hbar v_F\sqrt{\pi n} \quad (4)$$

where $v_F \approx 10^6$ m s^{-1} is the Fermi velocity of graphene and $\hbar$ is the reduced Plank constant.[12,18] The modulation of graphene Fermi level with V_{GS} ($E_F = 0$ eV at V_{CNP}) is plotted in the right y-axis of Figure 3h. We observe a change in pristine graphene Fermi level $\Delta E_F \approx 500$ meV whereas the maximum change in the zero-bias graphene/C_{60} energy barrier is $\Delta\phi_B \approx 660$ meV. This specific value of ΔE_F is the result of Equation (4), which as discussed earlier, might not be strictly valid in this context. However, the trend observed is interesting for a qualitative comparison with other devices reported in the current literature.[12,13,15,22,23]

Figure 4a shows the transistor behavior or I_{DS}–V_{GS} characteristics of the graphene/C_{60}/Al VFET at RT and at several positive V_{DS} (which corresponds to a reverse biased graphene/C_{60} junction). Here below we empirically extract meaningful parameters for the comparison of our devices with standard transistors. The transistor switches from the "off" state to the "on" state when V_{GS} is varied from −30 V to 70 V providing an on/off ratio up to ≈8×10^4 at $V_{DS} = 5$ V. The effective turn-on gate voltage (V^*_{GS} at which the transistor switches from "off" state to "on" state) gradually shifts from −4 V to −16 V as V_{DS}

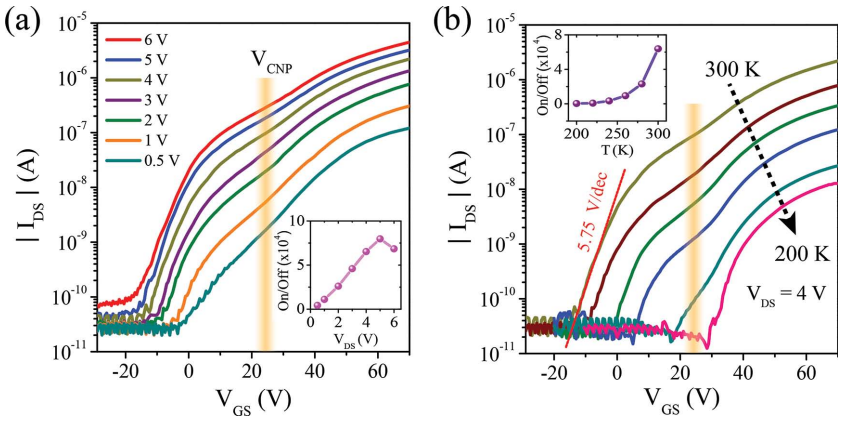

Figure 4. a) The reverse-biased diode current versus V_{GS} plots at several positive V_{DS}. Corresponding current on/off ratio are shown in the inset. b) The reverse-biased current versus V_{GS} plots of the same diode at V_{DS} of 4 V and at different temperatures from 300 to 200 K. The inset represents the corresponding change in current on/off ratio. The orange line in both (a) and (b) are just a guide-to-the-eye to mark the step observed around the graphene CNP.

is increased. In addition, a step-like feature of small current modulation is observed around $V_{GS} \approx 23$ V in all the transfer curves which directly correlates to the very small DOS (there is thermal broadening, otherwise it would have zero DOS) around the CNP of graphene. The measured "off" state current in our devices is as low as $\approx 2 \times 10^{-11}$ A and limited by a comparable gate leakage-current.

We carried out further temperature dependent measurements, which are shown in Figure 4b. The "off" state current is limited by the gate dielectric and shows very small temperature dependence. The "on" state current decreases very rapidly with decreasing temperatures due both to the reduction in C_{60} conductivity and to the reduction in the thermionic emission at the graphene/C_{60} junction. As expected, the current on/off ratio is higher at room temperature (see inset of Figure 4b). All these features are the consequence of the reduction of the kinetic energy of the electrons by reducing its temperature. To characterize the switching on the transistor we extract the subthreshold swing, i.e., the required V_{GS} for a tenfold change in I_{DS}. As indicated in Figure 4b, the value is estimated to be ≈ 5.75 V dec^{-1} and could be improved in a first approximation by lowering the thickness of the SiO_2[36] and/or using a high-κ dielectric.

After having studied the VFET operation in a graphene/C_{60} device, we focus on the optical characterization of the graphene/C_{60} phototransistor device. The top electrode is changed from Al to Cu in order to demonstrate similar VFET working principle in both devices. **Figure 5**a,b shows the I_{DS}–V_{DS} characteristics at RT in a graphene/C_{60}/Cu-based transistor in the dark and (I^*_{DS}–V_{DS}) under illumination, respectively. The light source is set at a constant intensity (≈ 1 kW m^{-2}) throughout the measurements to obtain the gate-modulated photocurrent under similar optical conditions. A large modulation in I_{DS} and I^*_{DS} is measured in the reverse bias condition of the graphene/C_{60} junction, i.e., at the positive V_{DS}, with an on/off ratio close to three orders of magnitude. Figure 5c shows the generated photocurrent, $I_{Ph} = I^*_{DS}(light) - I_{DS}(dark)$, versus V_{DS} plots at several V_{GS}. The I_{Ph}–V_{DS} curves resemble the I_{DS}–V_{DS} curves (with and without light), showing how the photo-generated carriers follow the diode characteristics. Figure 5d presents the photocurrent versus V_{GS} plots at several positive V_{DS}. The I_{Ph} modulation exceeds two orders of magnitude at around the CNP of the graphene strip and saturates at both large positive and negative gate voltages. Using the previous data of zero-bias energy barrier across the graphene/C_{60} junction, we can now

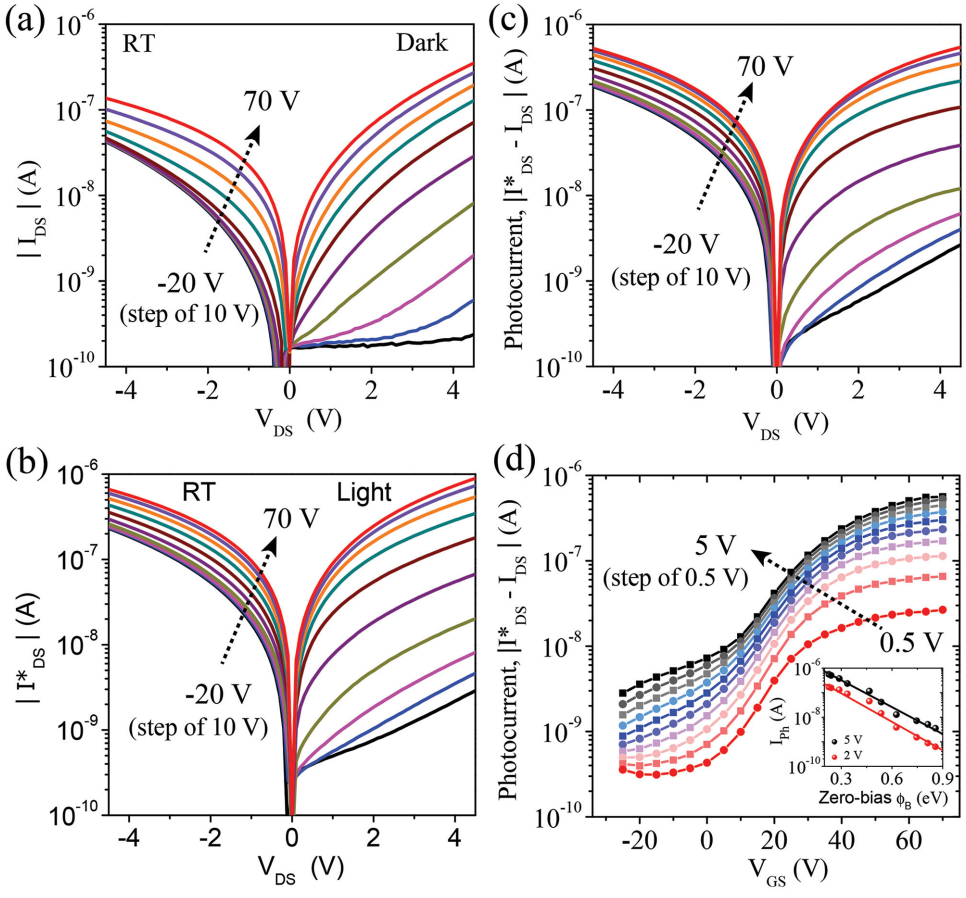

Figure 5. RT I_{DS}–V_{DS} characteristics in the Gr/C_{60}/Cu VFET at various fixed V_{GS} in a) dark and b) illuminated states. One Ti/Au contact to the graphene strip is grounded and the Cu electrode is biased. c) Photocurrent (I_{Ph}) versus V_{DS} plots at several fixed V_{GS}. d) Gating response of the photocurrent (I_{Ph}–V_{GS}) at several positive V_{DS}. The inset shows the dependence of the I_{Ph} at V_{DS} of 5 and 2 V with the zero-bias energy barrier of the graphene/C_{60} junction. The lines are fits to the equation $I_{ph} = \alpha \times exp(-\beta\phi_B)$, where α, β are the fitting parameters, with values $\alpha = 4.1$ μA, $\beta = 8.4$ V^{-1} for $V_{DS} = 5$ V and $\alpha = 1.4$ μA, $\beta = 8.9$ V^{-1} for $V_{DS} = 2$ V.

represent the photocurrent with respect to ϕ_B [Figure 5d, inset] where there is a clear exponential dependence. Our results confirm a large gate modulation of the photocurrent in graphene/C_{60}/Cu device (following previous results in related devices[37,38] and suggest an exponential dependence between the generated photocurrent and the graphene/C_{60} junction energy barrier.

3. Conclusions

In conclusion, we have shown a graphene/C_{60} fullerene device in which the interfacial energy barrier can be tuned by an applied gate voltage. Accordingly, the device can perform either as a highly rectifying diode or as a nonrectifying low resistance junction, which can be used for efficient charge carrier injection into (or extraction from) the molecular semiconductor. This result opens up the possibilities for graphene to be used as a potential electrode which works beyond the conventional "energy barrier limitation" in metal/molecular semiconductor junctions. The graphene/C_{60}/metal VFET, with a current on/off ratio of up to five orders of magnitude, can also be used as an alternative device scheme that circumvents the zero band gap limitations of a standard graphene FET. Moreover, the VFET shows a gate-modulated photocurrent which is exponentially dependent with the gate-controlled graphene/C_{60} energy barrier, which foresees the applicability of the graphene/molecular semiconductor junction in developing the field of light signal detection.

4. Experimental Section

The graphene/C_{60}-based VFETs are fabricated in two steps. In the first step, a standard graphene FET is fabricated and characterized before the organic layer deposition. Then the fullerene (C_{60}) and the top electrode are deposited to obtain the final VFET device in the next fabrication step. For the graphene FET fabrication, a large-area high-quality CVD-grown graphene is carefully transferred onto a 1×1 mm^2 Si/SiO_2 (300 nm) substrate (used as received from Graphenea S.A.). Several 2 mm long and 10 μm wide graphene strips are protected by polymethyl-methacrylate (PMMA) patterned by e-beam lithography and the rest of the graphene film is etched by oxygen plasma. The Ti/Au (2.5/40 nm) contacts are evaporated at the two ends of each graphene strips with a separation of 1.4 mm. The graphene FET is then electrically characterized in a variable-temperature high vacuum probe station (Lakeshore) with a Keithley-4200 semiconductor analyzer. After characterization, the next deposition steps for completing the VFET are carried out in a UHV dual chamber evaporator (base pressure $<10^{-9}$ mbar). The C_{60} layer is evaporated in one of the chambers from a Knudsen cell at a rate of 0.1 Å s^{-1}. The 280 nm thick C_{60} layer is evaporated in cross-bar geometry through the shadow mask in such a way that the C_{60} layer covers a graphene length of 1 mm. As the top electrode, a 30 nm thick layer of either Al or Cu is e-beam evaporated in the second chamber at a rate of 1 Å s^{-1} (starting from a slower rate of 0.4 Å s^{-1}) through another shadow mask in an overlapping area of 10×300 μm^2 between the graphene strip and the top electrode. The devices are then quickly transferred to the variable-temperature probe station for further electrical and optical measurements. For optical experiments, we use a commercial light source from SCHOTT GmbH.

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